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PROVISIONAL APPLICATION COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

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1. INVENTOR(S)

Given Name *(first and middle [if any])*	Family Name or Surname	Residence *(City and either State or Foreign Country)*
MOHAMED	AZIMANE	EINDHOVEN, THE NETHERLANDS

2. TITLE OF THE INVENTION

A NEW EFFICIENT SOLUTION TO COVER RESISTIVE-OPEN DEFECTS FOR SEMICONDUCTOR MEMORIES

3. CORRESPONDENCE ADDRESS

Philips Electronics North American Corporation
Intellectual Property & Standards
1109 McKay Drive, M/S-41SJ
San Jose, California 95131
Phone: (408) 474-9073
Fax: (408) 474-9082

24738
PATENT TRADEMARK OFFICE CUSTOMER NUMBER

4. ENCLOSED APPLICATION PARTS

- ☒ Specification **(8 pages)**
- ☒ Drawing(s) **(0 sheet(s))**
- ☒ Return-Receipt Postcard

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Respectfully submitted,

By Peter Zawilski

Peter Zawilski, Reg. No. 43,305
(408) 474-9063

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A New Efficient Solution to Cover Resistive-Open Defects for Semiconductor Memories

Mohamed Azimane
18 September 2003

Abstract

The invention describes a new and efficient solution to cover resistive-open defects for semiconductor memories. The solution will highly increase the delay faults coverage because it will enhance the stress of the sensitization operation using a determined set of test patterns. The delay faults are mainly due to the resistive open defects which leads to slow-to-rise and slow-to-fall behaviour at the memory address decoder, the pre-charge circuitry, the write data lines, the global inputs/outputs, and also in the matrix. This invention will compensate the fault coverage loss of testing at lower frequency than that of the memory.

1. Problem statement

Nowadays, embedded semiconductor memories are operating at high speed. The clock cycle reaches already 2 ns for SRAMs, which means that writing and reading from the memories needs only 2 ns of time, even less for the new generation of CMOS 90 nanometers. Testing the embedded memories is usually done with BIST (built-in-self-test) or with a tester using scan test mode. The BIST (or tester) generates consecutive test patterns to perform read and write operations at the memory, according to the family of the march test which are usually very known as the best way to test semiconductor memories. Other test patterns (Patent EP0738418 B1, ID NL030587) proof also high fault coverage to detect stuck-open defects and slow to rise and slow to fall at the address decoder.

The resistive open defects may not cause only static faulty behaviour, which are obviously easily to be detected. It may cause also dynamic faulty behaviour which is known as slow to rise and slow to fall either in the data path or the address path. Depending on the resistance value of the defect (defect size), these delays vary between small delays and big delays. The big delays are easily detected because it can be mapped to the static faulty behaviour. The small delays require high speed testing using the BIST or scan test to be detected. Ideally, the memories have to be tested at the operation frequency. For instance, a memory that operates at 200 MHz must be tested at the same frequency. Otherwise, many resistive open defects, resistive bridges and capacitive coupling faults will escape the test, even with the correct test patterns. Moreover, the high speed BIST can not be easily performed and included with the memory layout, either because of the extra area overhead, the delay needed for the output analyzer of the BIST, or because of the extra-time needed for the synthesis. Increasing the speed of the BIST implies extra area overhead that is unacceptable for the memory customers. They require high quality testing with small BIST area.

Testing the embedded memories using scan test mode is still a valid option, however this solution requires an extra test time due to the scan-in and the scan-out of the data, which is done in seri, therefore, this solution highly increases the test time for big memory sizes and for instances with high number of pins.

The resistive open defects are becoming the dominant defects due to the change from Aluminum backend to Cupper backend. In Aluminum backend (up to CMOS 18), the resistive bridges are more dominant than resistive opens. In Cupper backend (CMOS 12 and below), resistive opens are more dominant than ever before. Therefore, the upcoming technologies will highly suffer from the resistive open defects.

Testing at lower speed than the operation frequency of the memories will lead to test escape of the resistive open defects and also of the resistive bridges and the capacitive coupling which behaves as delay faults.

2. Disadvantages

The resistive open defects are becoming the dominant cause of the customer returns due to the dynamic faulty behaviour. Testing at lower frequency than that of the memory will cause low defect coverage and test escape. This problem will highly increase the customer returns because of the change to Cupper backend.

Applying the correct test patterns at lower frequency than that of the memory using BIST or scan test is not sufficient to cover the resistive open defects. The correct test patterns must be combined with the correct stress conditions in order to sensitize correctly the delay faults. In the case of the resistive open defects (or delay faults in general), it is already very known that high speed testing must be combined with the correct test patterns to reach high fault coverage. Testing at lower speed than that of the memory will lead to low fault coverage of the delay faults and therefore to customer returns.

3. Proposed solution

The BIST frequency has a significant impact on the fault coverage. The high speed testing increases the delay fault coverage because it detects the small delay faults caused by the resistive open defects. Testing the memories at lower frequency than the operation frequency will lead to test escape and reliability issues. To increase the fault coverage, the BIST should run at high speed. However, this requirement will lead to an extra area overhead. The synthesis of high BIST frequency is not always feasible due to different obstacles.

What the BIST (tester) is doing?

The BIST (tester) is an engine that generates the corresponding addresses and data background, and runs consecutive read and write operations in increasing and decreasing address order. In case of read operation, the output analyzer of the BIST compares the read out data with the expected logic values. If they match then the memory is fault free, otherwise, the memory is faulty.

To perform this test, the BIST delivers the addresses and data background to the memory and then runs the positive edge of the clock, which arrives to take action on the memory depending on the write enable signal (read or write).

Process steps of the BIST (tester):

1. Generates the address and data background depending on the march test,

2. Hold state, then the address and data bits become valid,
3. Deliver the address and data background to the memory inputs,
4. Positive edge of the clock will start the memory operation (read or write),
5. Depending on the write enable signal, the data background will be written to the memory, or will be read out and compared with the expected logic values.

These steps are repeated depending on the complexity of the test patterns and the memory size. The end of testing is reported by the BIST (tester) when a ready signal is delivered and a second flag shows either the device under test is faulty or fault free.

Figure 1 shows the waveforms of the address and data generation with the memory clock. We define the address and data set-up time as the time that exists in between the address and data background generation and the positive/negative edge of the clock.

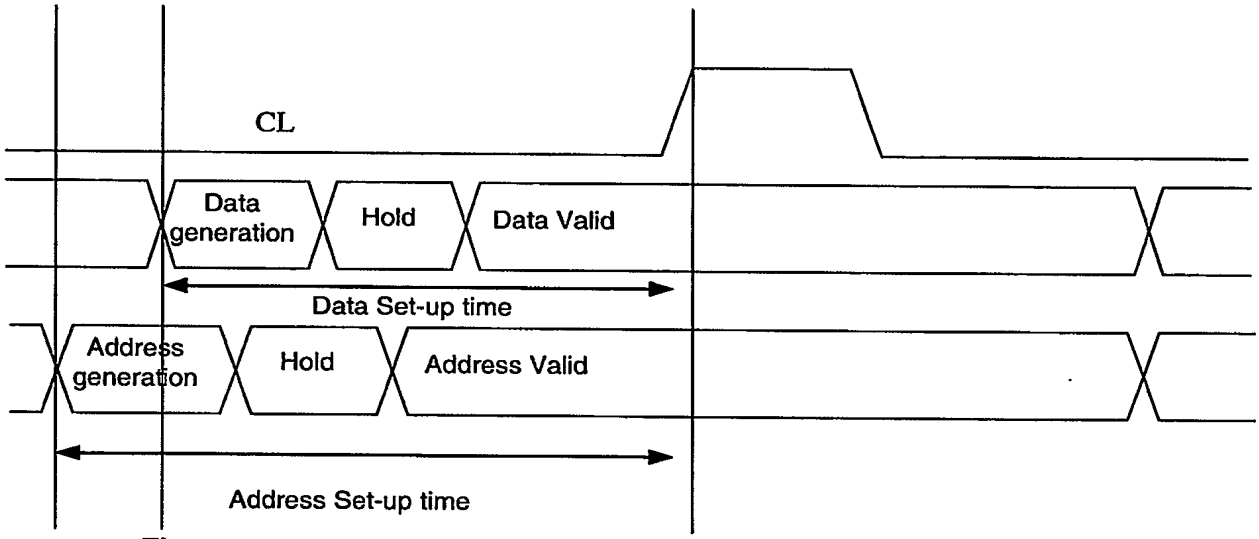

Figure 1: Data set-up time and address set-up time during the data and address generation in a BIST.

The address and data background generation may run at lower frequency than that of the memory. Thus, the delay faults are masked when these test patterns (address and data bits) are delivered to the memory inputs for a quite long time before the positive edge of the clock. For BIST (tester) that runs at 50 MHz, it needs 20 ns to perform read/write operation. These 20 ns are needed for address and data background generation, and then data comparison for the output analyzer in case of read operation. In this case, an amount of time of 10 ns is needed to generate and deliver a set of address bits and data bits to the memory inputs. Suppose that a memory is operating at 2 ns clock cycle, if the address and data background are delivered to the memory for about 10 ns before the positive edge of the clock, the periphery circuitry is already in very stable state before the positive edge of the clock. Any resistive open defect at the memory periphery will survive during the application of the test pattern because a delay of 10 ns before the positive edge of the clock will obviously mask the fault effect.

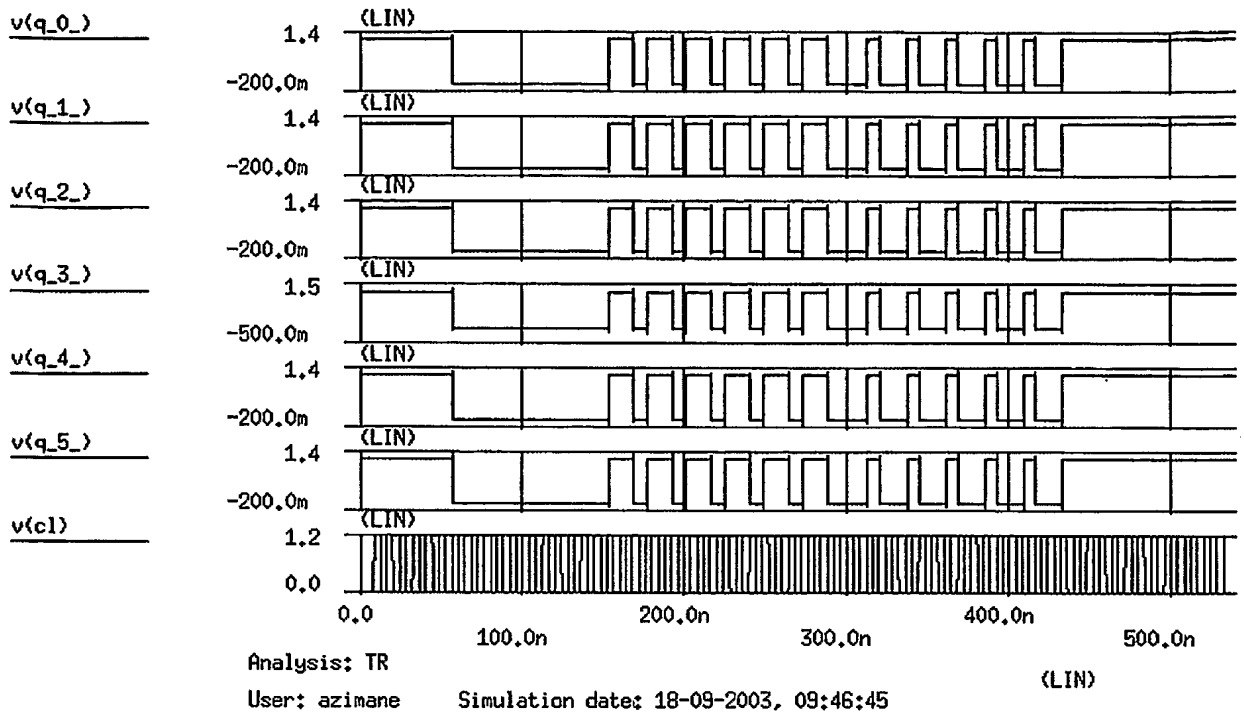

Figure 2: Golden Simulation results of a RAM using a march test.

Nowadays, the memories are self-timed. An internal clock is generated based on the rising or the falling edge of the external clock. The internal clock is then controlling the read/write operations. The self-timing techniques avoid an incomplete read or write operation to occur. For testing delay faults, the state of the circuit before the positive/negative edge of the internal clock is critical. The small delay faults are detected when the state of the circuit is not yet stable due to the delay fault. When the rising edge of the external clock is on time, the internal clock of the memory is generated and the circuit is still not yet stable. Thus, the delay fault has an impact on the memory behaviour and then is detected. Therefore, the set-up time that separates the positive or the negative clock edge and the delivery of the memory inputs is very critical.

When the both the address and data set-up time is high with respect to the memory clock cycle, then the address decoder, the write circuitry, the sense amplifiers, the precharge and the discharge circuitry are already stable before the positive/negative edge of the clock gives the beginning of the read/write action. Thus, the delay faults will not be detected because the periphery is already on stable state. The delay faults will have no impact on the faulty behaviour.

As follows simulation results are given to show the difference between the impact of the set-up-time on the memory behaviour. Figure 2 shows the golden simulation result of a memory net list with six output pins q[0..5]. This Figure is the simulation result of a very know march test highly used with Philips and is already known with high fault coverage. The memory can operate at 2 ns clock cycle, while the BIST runs the march test at 50 MHz, which means 20 ns clock cycle. Thus, the address and data set-up time is around 10 ns.

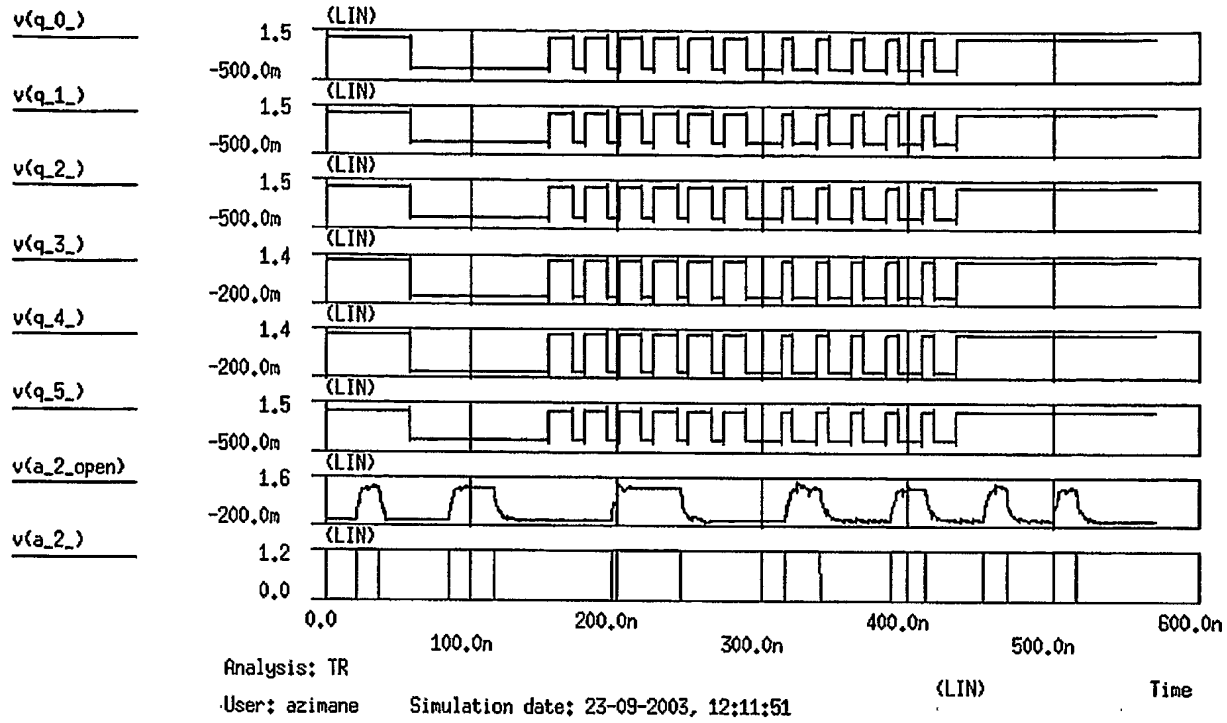

Figure 3: Simulation results of faulty net list with an injected open defect at the least significant bit of the X address decoder

Figure 3 shows the simulation result of the same net list at the same stress conditions with an injected open defect at the least significant bit of the X address decoder. This open defect behaves as slow-to-rise as shown in the waveform of the V(a_2_open). Figure 4 shows a zoom of small frame time of the same simulation. The memory operates as the pin a_2_ reaches the logic value one 5 ns later, however, this memory must operate at 2 ns clock cycle. Therefore, this defect will obviously escape the test when the BIST (tester) runs at lower frequency than that of the memory.

By reducing the set-up time in between the address generator and the memory inputs, either by shifting the positive edge of the clock or the address validation, the delay faults at the address decoder will be easily detected. The same applies for the data background. This includes also the self-timed memories, because both the address decoder and the write circuitry will fail by changing the set-up time.

Instead to synthesis the BIST at very high frequency which increases the BIST area, we could reduce the set-up time in between the delivery of the address bits and the data bits to the memory inputs and the positive edge of the external clock.

For instance, a memory that runs at 200 MHz must be tested at the same frequency, otherwise, the fault coverage loss is increased and this will lead to ship a faulty chips. Testing this memory at 50 MHz or even at 150 MHz will not cover completely the resistive open defects. The solution to resolve this fault coverage loss is by reducing the set-up time in between the data generation and the address generation and the positive edge of the clock. By reducing this gap, both the address

decoder and the write circuitry will be stressed in time, even for the self-timed memories.

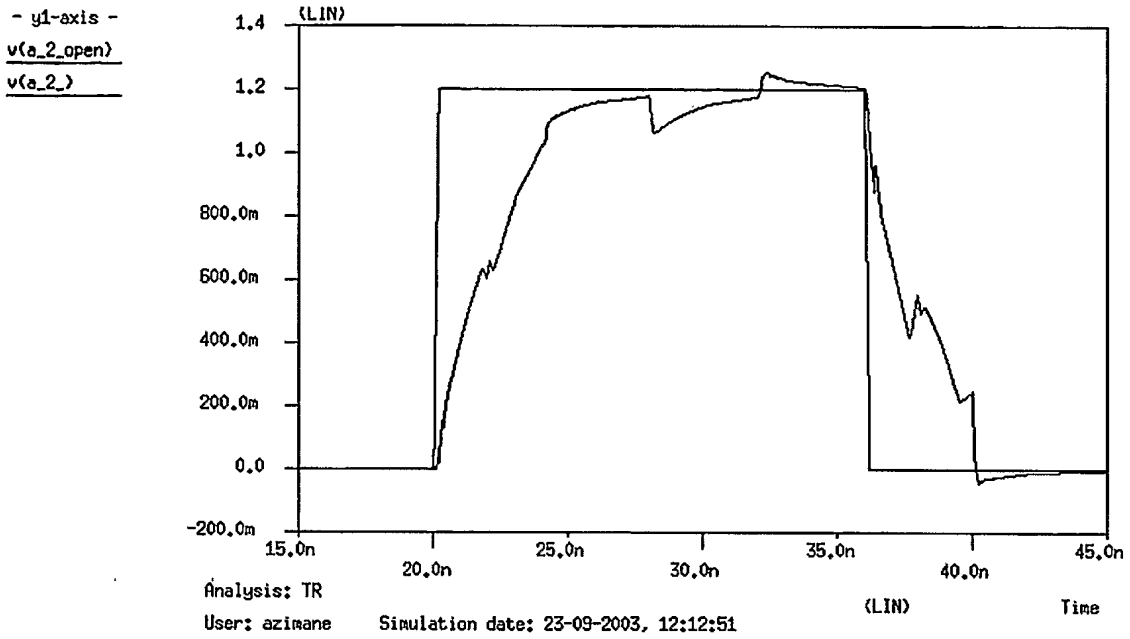

Figure 4: Slow to rise and slow to fall at the least significant pin of the X address decoder due to resistive open defect

To resolve this fault coverage loss, the set-up time for both the address bits and the data bits must be reduced. This will highly stress both the address decoder and the read/write circuitry. When a high speed testing becomes costly, the solutions to resolve the fault coverage loss is by synthesizing the BIST at the maximum possible acceptable frequency (trade off area overhead v frequency), and the gap can be compensated by reducing the set-up time.

Figure 5 shows the simulation result with reduced address set-up time of the same faulty net list and the same test bench (same march test). The simulation shows that the defect is detected when the set-up time between the address bits and the positive edge of the clock is reduced. The memory outputs q_1_ and q_2_ gives unexpected logic values at 50 ns, while all the memory outputs give the wrong logic value at 240 ns.

This technique has the same effect as the high speed testing to cover delay faults. This simulation shows clear evidence that testing the same device with the same test patterns and with smaller set-up time will lead to high fault coverage of the delay faults. It shows also that testing with high set-up time has the same effect as the low speed testing.

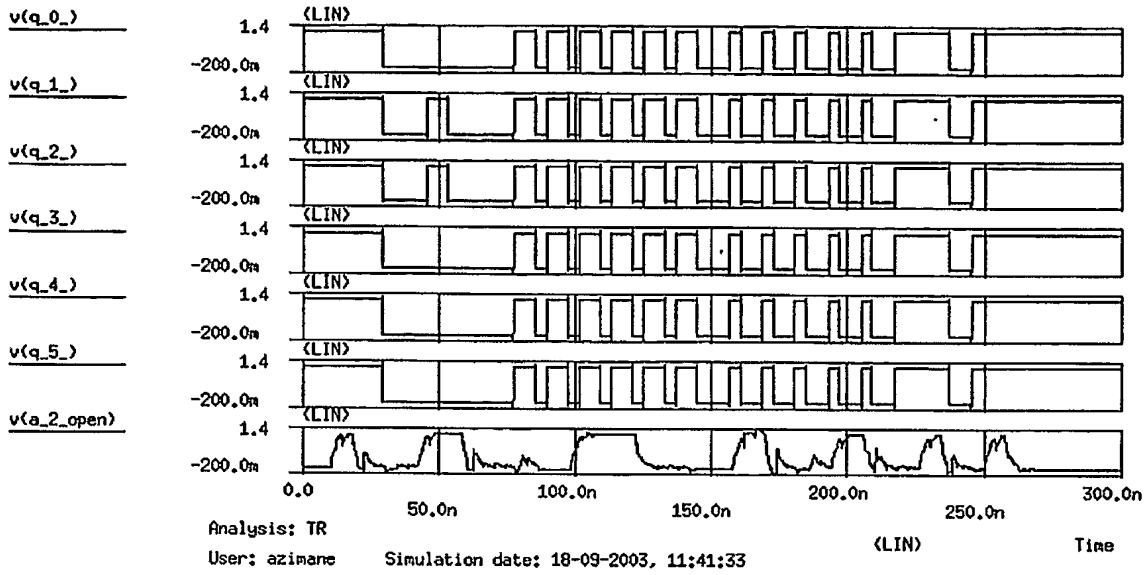

Figure 5: Reduction of the address set-up time shows a detection of the resistive open defect during two different clock cycles.

4. Advantages

This solution will highly increase the resistive open defect coverage, because it stresses in the time domain the memory periphery, even for the self-timed memories. The slow to rise and the slow to fall defect coverage will be highly increased by only reducing the address and data set-up time.

This invention shows that the set-up time is the key to increase the delay fault coverage when the BIST (or tester) operates a lower frequency than that of the device under test. This technique will compensate the fault coverage loss due to the low frequency testing. These timing issues must be combined with the correct test patterns needed to detect the delay faults in semiconductor memories. Applying the correct test patterns at lower frequency than that of the memory will lead to test escape. The fault coverage is increasing when the correct test patterns are combined with the set-up time conditions described in this invention.

5. Background material

EP0738418 B1 G11c 20020116 Koninklijke Philips Electronics N.V. "*A method of testing a memory address decoder*".
[Azimane 01] M. Azimane, "New Test Methods to Detect Address Decoder Delay Faults in ROM", Nat.Lab. Technical Note 7176.

[Sachdev 97] M. Sachdev, "*Open Defects in CMOS RAM Address Decoders*", IEEE Design & Test of Computers, April-June 1997, pp. 26-33.
[Otterstedt 98] J. Otterstedt, D. Niggemeyer and T. W. Williams, "*Detection of CMOS Address Decoder Open Faults with March and Pseudo Random Memory Test*", in Proc. Int'l Test Conf., Oct. 1998, pp. 53-62.